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METHOD TO AVOID A LASER MARKED AREA STEP HEIGHT

FIELD OF THE INVENTION

001 This invention generally relates to semiconductor processing methods including photolithographic patterning and more particularly to a method for forming laser marked areas to avoid a defocusing step height with respect to adjacent active areas of a process wafer in addition to reducing accumulation of CMP residue over the laser mark area to improve subsequent manufacturing processes.

BACKGROUND OF THE INVENTION

002 As device critical dimensions shrink to lower than deep submicron (less than 0.25 micron), the efficient use of wafer process area becomes critical. The practice in the industry has been to add a laser mark consisting of an alphanumeric, barcode, or other type of identification mark on the front of process side of the wafer to characterize e.g., the wafer manufacturer, conductivity type, resistivity, flatness, wafer number, and device type. Automatic code readers can track the process wafers at various stages of the process and provide information on wafer movement in the fabrication process. The wafer laser

mark is typically located at the wafer periphery in an exclusion zone that is within about 2 to about 3 mm from the wafer peripheral edge.

003 In a typical integrated circuit manufacturing process, photolithographically formed patterns and etched features are formed across the entire wafer, including the exclusion zone to reduce subsequent CMP preferential polishing in unpatterned areas, also referred to as a CMP loading effect.

004 According to prior art processes, in order to avoid covering up the laser mark at the wafer periphery, the practice has been to remove resist overlying the laser mark area to allow the material above the laser mark to be cleared out in a subsequent etching process.

005 A problem with prior art approaches is that by removing material over the laser mark area an undesirable step height is formed between the process surface and the laser mark area resulting in loss of resolution of neighboring formed feature patterns in lithographic processes due the phenomenon of defocus. The rejection of neighboring die areas is costly to yield. Further, the recessed area in the wafer process surface created by the cleared out laser mark area will act as a trap

for collecting metal residue, for example copper, in subsequent integrated circuit manufacturing processes, increasing the possibility of wafer contamination including cross-process particle contamination.

006 Therefore, there is a need in the semiconductor processing art to develop an improved method for preserving process wafer laser markings while avoiding detrimental effects including loss of pattern resolution in neighboring active die areas.

007 It is therefore among the objects of the present invention to provide an improved method for preserving process wafer laser markings while avoiding detrimental effects including loss of pattern resolution in neighboring active die areas, while overcoming other shortcomings of the prior art.

SUMMARY OF THE INVENTION

008 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a method for avoiding a step height over a readable

laser marked portion of a process wafer to improve a subsequent patterning process of adjacent active areas.

009 In a first embodiment, the method includes providing a process wafer comprising active area trenches and at least one inactive area trench formed overlying at least a portion of a laser marked portion; forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches; forming a resist layer comprising patterned portions disposed between the active area trenches and the at least one inactive area trench; removing the filling layer portions not covered by the resist layer; removing the resist layer; and, planarizing the wafer process surface wherein the active area trenches and the at least one inactive area trench are substantially co-planar.

0010 These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

0011 Figure 1A is a top planar view of an exemplary semiconductor wafer laser marked area adjacent active area die according to an embodiment of the present invention.

0012 Figure 1B is an expanded top planar view of an exemplary semiconductor wafer laser mark area including a dummy pattern according to an embodiment of the present invention.

0013 Figures 2A-2H are cross-sectional views of a portion of a process wafer at stages in manufacture of STI structures according to an embodiment of the present invention.

0014 Figure 3 is a process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

0015 Although the method of the present invention is explained in exemplary implementation with respect to an STI formation process, it will be appreciated that the method of leaving resist covering a laser mark area, while forming a dummy pattern

between an active device area and a laser mark area prior to an etching process to improve a subsequent CMP process may be used to avoid a step height in other device formation processes, for example to prevent a step height over an alignment mark area. The term 'active area' as used herein refers to areas of the semiconductor process surface where electrically active areas are formed as integrated circuit components of a semiconductor device, for example including one or more die areas of the wafer.

0016 For example, referring to Figure 1A is shown a top planar view an exemplary semiconductor process wafer 12 having a laser mark area, e.g., 14 located at a periphery of the process wafer, for example an exclusion zone or inactive area of the wafer and having adjacent active area dice, e.g., 16A, 16B, and 16C. The laser mark area 14 may be any conventional laser mark area, where a process wafer information is added by conventional methods of laser marking in the exclusion zone during a wafer preparation process, for example in an area between about 2mm and about 4mm from the wafer peripheral edge. The wafer laser markings include, for example, alphanumeric, barcode, or other type of identification marks on the process side of the wafer to

characterize e.g., the wafer manufacturer, conductivity type, resistivity, flatness, wafer number, and device type.

0017 It has been found according to the present invention that a lithographic patterning process carried out over active areas adjacent the laser mark area 14, e.g., an active area encompassed by circle 15, is improved by eliminating a step height over the laser mark area in an STI formation process according to an embodiment of the invention. For example it has been found that adjacent an adjacent active area including several die portions of the wafer, e.g., those die within circle portion A, suffer from a defocusing effect in a photolithographic process due to a laser mark step height according to prior art processes. The present invention, by eliminating the step height over the laser mark area 14, solves the defocusing problem and improves lithographic patterning resolution for die adjacent the laser mark area, e.g., within circled wafer portion A.

0018 For example, referring to Figure 1B, is shown a top planar view of an expanded portion of the exemplary laser mark area 14 including an adjacent active area e.g., die portions

16A, 16B, and 16C. In an exemplary embodiment of the present invention as explained in greater detail in Figure 2A - 2F, a dummy pattern e.g., lines 18A, 18B, and 18C are formed between the active device areas, e.g., 16A, 16B, and 16C, and the laser mark area 14, prior to a CMP process to form backfilled shallow trench isolation (STI) structures. Preferably, the dummy pattern is formed at least adjacent the full length L of the active device areas of the process wafer. In addition, the width W, of the dummy pattern is greater than about 1.5 mm, which may include one or more lines, preferably two or more lines, preferably about evenly spaced,

0019 For example, the individual linewidths e.g., 18A, 18B, and 18C of the dummy pattern may be formed with a linewidth of from about 1 micron to about 500 microns and with a pitch (spacing between lines) a factor of about 1 to about 4 times the linewidth. It will be appreciated that the linewidths and overall width, W of the dummy pattern may be varied depending on the area between the active device area e.g., 16A, 16B, and 16C and the laser mark area 14.

0020 Referring to Figure 2A, is shown an exemplary process wafer cross sectional view according to in an exemplary implementation of the method of the present invention. Shown is a silicon wafer substrate 22, preferably having a thermally grown pad oxide (e.g., SiO_2) overlayer (not shown) and an overlying nitride layer, preferably a silicon nitride (e.g., Si_3N_4) and/or silicon oxynitride (e.g., SiON) hardmask layer 24 formed by conventional processes, e.g., LPCDV or PECVD to conventional thicknesses, for example from about 500 Angstroms to about 2000 Angstroms.

0021 Still referring to Figure 2A, a resist layer e.g., 26 is deposited and patterned according to conventional process to form an etching pattern e.g., openings 26A and 26B for forming STI trenches (active area trenches) in the silicon substrate 22 and including an arbitrary pattern at the wafer periphery overlying a wafer laser marked area 28, generally represented in cross section by enclosed box area 22B.

0022 Referring to Figure 2B, a conventional localized (edge removal) stripping process is used to remove the resist layer 26

portions overlying the wafer peripheral exclusion area (inactive area) e.g., 28A including overlying the laser mark area 28 for forming a trench (inactive area trench). Referring to Figure 2C, a conventional plasma enhanced etch process is then carried out to first etch through the overlying nitride hard mask layer 24, followed by a conventional plasma enhanced silicon etching process to form STI trenches e.g., 30A, 30B in the active device region in the silicon substrate 22 as well as a trench e.g., 30C overlying the laser mark area 28. The STI trenches are formed to conventional depths and widths, for example, having sidewall angles between about 70 and about 85 degrees.

0023 Referring to Figure 2D, following optionally thermally growing an oxide liner (not shown) within the STI trenches, the trenches are backfilled with SiO_2, also referred to as an STI oxide by a conventional blanket deposition process, e.g., HDP-CVD or PECVD, preferably HDP-CVD. It will be appreciated that the surface topography following the blanket deposition process is schematically represented in the Figures. For example, STI oxide layer 31 is shown as nonplanar process surface topography following the blanket deposition process. Preferably the STI oxide layer is backfilled to about equal to or higher than the

nitride hardmask layer 24 to produce backfilled trenches e.g., 31A, 31B, and 31C.

0024 Referring to Figure 2E, in an aspect of the present invention, a reverse mask etch process, also referred to as a reverse tone patterning process is carried out to form a patterned photoresist layer over the STI oxide layer 31, leaving resist layer portions e.g., 32A and 32B overlying the STI trenches in the active device area of the wafer. In an important aspect of the invention an undeveloped resist layer portion e.g., 32C is left overlying a portion of an inactive area at the wafer periphery. The inactive area covered by the resist portion e.g., 32C preferably includes an area adjacent to the active area including STI trenches e.g., 31A, and 31B disposed between the laser mark area of the wafer and the STI trenches including overlying the laser mark area 28, e.g., extending up to about the wafer peripheral edge (not shown).

0025 Referring to Figure 2F, in another aspect of the invention, following the reverse tone patterning process including development of the resist, a dummy pattern is added to unpatterned resist portion e.g., 32C between the active area

including STI trench 31B and the inactive area trench 31C overlying the laser mark area 28. For example, following the reverse tone patterning process, an additional dummy pattern mask, according to preferred embodiments, is interposed between the reverse tone pattern mask and the process wafer surface to allow proper re-alignment of the reticle (mask) over the desired wafer exposure area, e.g., a one shot exposure of resist portion 32C, while avoiding shadowing (shielding) effects from the reverse tone pattern mask during exposure. Following exposure and development of the resist layer portion 32C, dummy pattern resist portions e.g., 32D and 32E are formed in the resist layer as shown in an exemplary embodiment, while leaving a portion of resist layer portion e.g., 32C overlying the trench 31C, which at least partially, preferably substantially completely, overlies the laser mark area 28.

0026 Referring to Figure 2G, a conventional STI oxide dry etching process is then carried to etch through the STI oxide layer thickness according to the patterned resist portions and expose the hard mask layer 24. Following removal of the reverse tone patterning resist layer portions by a conventional resist removal process, unetched portions of the STI oxide layer, e.g.,

underlying resist pattern portions 32D and 32E, e.g., 34A and 34B, respectively remain as a dummy pattern. Advantageously the dummy pattern portions of the STI oxide layer e.g., 34A, 34B, act to prevent CMP loading, or preferential polishing of both the active area and adjacent inactive area in a subsequent CMP process.

0027 Referring to Figure 2H, following removal of the resist layer portions, a conventional STI oxide CMP process is then carried out to remove remaining portions of the STI oxide layer, stopping on the hardmask layer 24. Advantageously, the filled trench 31C overlying the laser mark area prevents collection of CMP residue and advantageously eliminates a step height in subsequent photolithographic patterning processes, thereby avoiding a defocusing effect to improve a resolution of subsequently patterned features in adjacent active areas e.g., between STI trenches 31A and 31B. It will be appreciated that the STI oxide overlying the laser mark area may optionally be removed in a subsequent process.

0028 Referring to Figure 3 is an exemplary process flow diagram including several embodiments of the present invention.

In process 301, a semiconductor process wafer including a laser mark area is provided including an uppermost hardmask layer overlying active areas and laser mark areas. In process 303 an STI trench photolithographic patterning process is carried out including exposing an area overlying the laser mark followed by an etching process to form STI trenches including a trench overlying the laser mark area (laser mark trench). In process 305, an STI oxide layer is deposited to backfill the STI trenches and laser mark trench. In process 307, a reverse tone patterning process is carried out to form reverse tone pattern resist portions overlying the STI trenches and an inactive area including the laser mark area. In process 309, a second patterning process is carried out to form a dummy pattern in the inactive area portion disposed between the active area STI trenches and the laser mark area according to preferred embodiments. In process 311, a dry etching process is carried out to etch through the STI oxide layer thickness to expose portions of the hard mask layer. In process 313, an STI oxide CMP process is carried out to remove residual STI oxide portions to planarize the wafer process surface including form a substantially co-planar laser mark area to eliminate a step height.

0029 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.